

IN THE  
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Barry J. Arnold

Confirmation No.:

Application No.:

Examiner:

Filing Date: Nov 28, 2003

Group Art Unit:

Title: PARTIAL TERMINATION VOLTAGE CURRENT SHUNTING

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- ☒ under 37 CFR 1.97(b), or  
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)
- ☐ under 37 CFR 1.97(c) together with either a:  
☐ Statement under 37 CFR 1.97(e), or  
☐ a \$180.00 fee under 37 CFR 1.17(p), or  
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)
- ☐ under 37 CFR 1.97 (d) together with a:  
☐ Statement under 37 CFR 1.97(e)(1) or (2), and  
☐ a \$180.00 fee set forth in 37 CFR 1.17(p).  
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

☒ Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. ET 464 278 362 US

Date of Deposit Nov 28, 2003

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450

By

Typed Name: Matthew C. Fagan, Reg. 37,542

Respectfully submitted,

Barry J. Arnold

By

Matthew C. Fagan

Attorney/Agent for Applicant(s)  
Reg. No. 37,542

Date: Nov 28, 2003

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR  
APPLICANT'S INFORMATION DISCLOSURE  
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.

200209117-1

APPLICATION NO.

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APPLICANT

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GROUP

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	5,254,883	Oct 19, 1993	Horowitz et al.	
	1B	5,338,979	Aug 16, 1994	Mammano et al.	
	1C	5,359,235	Oct 25, 1994	Coyle et al.	
	1D	5,420,525	May 30, 1995	Maloberti et al.	
	1E	5,528,167	Jun 18, 1996	Samela et al.	
	1F	5,576,642	Nov 19, 1996	Nguyen et al.	
	1G	5,721,875	Feb 24, 1998	Fletcher et al.	
	1H	5,819,099	Oct 6, 1998	Ovens	
	1I	5,959,481	Sep 28, 1999	Donnelly et al.	
	1J	5,966,042	Oct 12, 1999	Werner et al.	
	1K	6,121,789	Sep 19, 2000	Liu et al.	

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L	EP0284356A2	28 Sep 1988	Ohshima et al.		
	1M					
	1N					
	1O					
	1P					

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Gabara, Thaddeus J., et al., "Forming Damped LRC Parasitic Circuits in Simultaneously Switched CMOS Output Buffers," IEEE Journal of Solid-State Circuits, Vol. 32, No. 3, pp. 407-418 (March 1997).
	1R	Ilkbahar, Alper, et al., "Itanium(TM) Processor System Bus Design," IEEE Journal of Solid-State Circuits, Vol. 36, No. 10, pp. 1565-1573 (October 2001).
	1S	

EXAMINER

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MCC  
11/28/2003

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EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	6,239,621	May 29, 2001	Milshtein et al.	
	1B	6,356,106	Mar 12, 2002	Greeff et al.	
	1C	6,448,837	Sep 10, 2002	Naffziger	
	1D	6,483,348	Nov 19, 2002	Naffziger	
	1E	2002/0084826	Jul 4, 2002	Naffziger	
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

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	1L					
	1M					
	1N					
	1O					
	1P					

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	
	1R	
	1S	

EXAMINER

DATE CONSIDERED